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Flexible complementary metal oxide semiconductor microelectrode arrays with applications in single cell characterization

H. Pajouhi,[1,2] A. Y. Jou,[1,2] R. Jain,[1,3] A. Ziabari,[1,2] A. Shakouri,[1,2] C. A. Savran,[1,3,4] and S. Mohammadi[1,2]

[1]*Birck Nanotechnology Center, Purdue University, 1205 West State Street, West Lafayette, Indiana 47907, USA*
[2]*School of Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907, USA*
[3]*School of Mechanical Engineering, Purdue University, West Lafayette, Indiana 47907, USA*
[4]*Weldon School of Biomedical Engineering, Purdue University, West Lafayette, Indiana 47907, USA*

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A highly flexible microelectrode array with an embedded complementary metal oxide semiconductor (CMOS) instrumentation amplifier suitable for sensing surfaces of biological entities is developed. The array is based on ultrathin CMOS islands that are thermally isolated from each other and are interconnected by meandered nano-scale wires that can adapt to cellular surfaces with micro-scale curvatures. CMOS temperature sensors are placed in the islands and are optimally biased to have high temperature sensitivity. While no live cell thermometry is conducted, a measured temperature sensitivity of 0.15 °C in the temperature range of 35 to 40 °C is achieved by utilizing a low noise CMOS lock-in amplifier implemented in the same technology. The monolithic nature of CMOS sensors and amplifier circuits and their versatile flexible interconnecting wires overcome the sensitivity and yield limitations of microelectrode arrays fabricated in competing technologies. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4935939]

Biological sensing at micro- and nano-scales facilitated by high performance electrodes leads to a better understanding of single cell behavior.[1] A variety of such electrodes have been developed to record electrical activities of beating cells, using both intracellular[2–5] and extracellular[6] techniques. A planar high-density microelectrode array (MEA) is an example of such electrodes utilized in an extracellular in-vitro measurement for interfacing to neurons.[7] Moreover, nanoscopic probes, such as nanopillar electrode arrays,[4,8] are extensively used for intracellular action potential measurement of individual neurons.[2] The weak nature of biological signals combined with three-dimensional moving surfaces of cells and tissues demand tight integration of an array of flexible electrodes with electronic amplifier circuits to enhance the recovery of such signals. While novel flexible electronic sensors with improved sensitivities have been developed, they still require a number of leads coming out of the sensor array and in some cases require external instrumentation amplifiers for signal recovery. Such designs not only lead to loss of the overall sensitivity and reduced measurement bandwidth but also demand complex integration and packaging approaches.[9] At the cellular level, three-dimensional kinked nanowire FETs have been proposed for single cell action potential recording.[5] The kinked nanowire based designs have achieved high sensitivity at the sensor level, but require external amplifiers with associated path loss and undesired coupling, compromising their overall sensitivity. At the tissue level, three-dimensional flexible circuits on deformable sheets that bend according to the curvatures of tissues, provide interface for in-vivo characterization.[10–12] While these techniques have utilized simple integrated electronics, they can benefit from large scale integration in order to reduce the distance among array sensors, further reducing the number of leads coming out of the array (analog multiplexing) and enhancing detected signals achieved by analog and digital signal processing and amplification.

Previously reported flexible electronic circuits are based on either thinned-down Si flakes that can only bend at a few millimeter radius to prevent damage[13] or transferred-printed silicon micro-islands,[14–16] presumably characterized with low yield as device density increases.[17] In this work, an ultra-flexible microelectrode array based on complementary metal oxide semiconductor (CMOS) ultrathin membranes is fabricated. The array can be easily laminated on micron-size curved surfaces such as the surface of a single cell, and is equipped with very dense electronics. To demonstrate the functionality of complex electronics on the array, CMOS temperature sensors and instrumentation amplifiers for precision single cell thermometry are implemented and tested. The operating conditions of CMOS transistors utilized as temperature sensors are optimized to enhance the measurement sensitivity.

Cell temperature is an indicator of cellular processes such as cell division, metabolism, and enzyme reaction.[18] For example, precision cell thermometry can identify cancer cells that are characterized with slightly higher temperatures than normal cells.[19] Additionally, the temperature across a single cell is not constant and is slightly elevated around mitochondrion due to their high metabolism. While accurate in-vivo measurement of temperature across a cell is important, understanding the behavior of a cell demands other sensors such as potential and pH sensors to be integrated within the flexible sensing platform. Such flexible microelectrode array with integrated sensors and electronic amplifiers will become an instrumental tool for understanding the cell behavior without disturbing its environment.

A standard CMOS technology (Global Foundries 45 nm Silicon on Isolator) that brings about reliability, reproducibility,

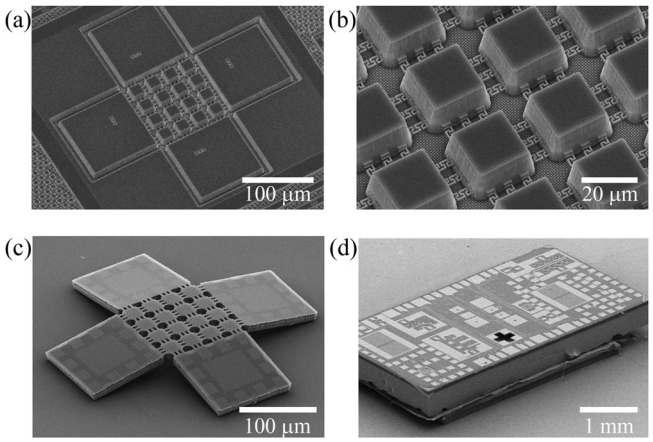

FIG. 1. SEM images of the microprobe array being etched and released during a post-CMOS processing technology. (a) The microarray structure on a CMOS SOI chip. (b) Microarray islands after the plasma etch and before the release. (c) Released microelectrode array. (d) Chip after the release of the microelectrode array.

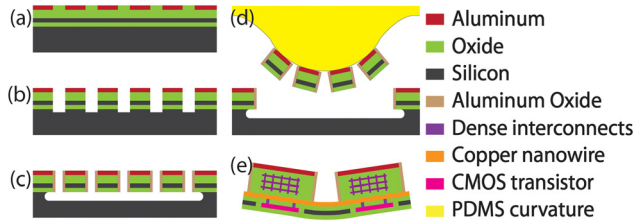

FIG. 2. Fabrication process flow: (a) CMOS chip after fabrication in the foundry. (b) Anisotropic dry etching using ICP. (c) Aluminum oxide deposition followed by ICP anisotropic etching and XeF_2 isotropic etching. The SOI Oxide layer (buried oxide) served as intrinsic etch-stop to protect the island from the bottom. (d) Transferring the array using PDMS transfer-printing technique. (e) Zoomed-in schematic of two cells of the array and the nanowire interconnects.

and large integration capability at low development costs is utilized in this work. Arrays of 4×4 ultrathin CMOS islands interconnected by meandered copper (Cu) metals are transfer-printed in one piece onto host substrates or cells, bypassing the yield-limiting obstacles of previously reported transfer-printing techniques for complex circuits.[17] As shown in Figs. 1(a) and 1(b), each island of the array is $19 \times 19\ \mu m^2$ with a thickness of about $10\ \mu m$ (A stack of 220 nm Silicon on Insulator (SOI) layer and a $\sim 10\ \mu m$ thick interconnection/oxide layer on top). The array is surrounded by four $90 \times 90\ \mu m^2$ pads. Each island is interconnected with 12 meandered copper wires, of which only four are connected to the input/output (I/O) pads. An alternative design with finer (70 nm metal width) and fewer meandered interconnects (4 wires for each Si island) is implemented as well. The microelectrode array can be scaled to much smaller dimensions, enabling characterization of several test points across the surface of a single cell with a diameter of a few μm. High density interconnect is achieved through utilizing a commercial 45 nm CMOS Silicon on Insulator technology with eleven layers of metallizations. With multitude of interconnection layers inside each island, integration of dense circuits such as amplifiers and signal processing circuits within each island is feasible. The integration of sensor and amplifier enables high signal-to-noise ratios and enhanced sensitivity.

CMOS islands are formed in a post-CMOS processing technology[20,21] based on a one-step dry isotropic etching without a need for lithography. The top aluminum metallization layer in the CMOS process serves as a built-in mask to form Si islands inside an Inductively Coupled Plasma (ICP) etcher. Ultrathin ($\sim 10\ \mu m$ thick) CMOS micro-islands are then suspended using Xenon di-fluoride (XeF_2) gas that etches the silicon substrate underneath the array. Sidewalls are protected with a thin layer of Al_2O_3 formed by atomic layer deposition, which also provides electrical isolation. Parameters such as pressure and gas duty cycle have been optimized by taking an infrared (IR) microscope image after each etching cycle. Fig. 2 summarizes the post processing steps and provides a cross sectional schematic of the islands and their interconnecting metals.

The two bottom copper layers in the CMOS technology are used to form the meandered interconnects, with widths of 400 nm and thickness of 870 nm for two metal layers and a low-K dielectric layer between them. The top copper layer serves as a mask in the isotropic etching process while the bottom copper layer acts as the conductive media among sensors/circuits and I/O pads. Meandered geometries for interconnections used in this work provide excellent flexibility.[22] On the other hand, thinning down the islands to $10\ \mu m$ of dielectric/metallization layer and only 220 nm Silicon on Insulator layer reduces the stress and leads to minimal strain bending and enhanced flexibility.[23]

The flexibility of the array was experimentally tested by applying a gentle force to the suspended array, using a computer controlled tip as illustrated in Figs. 3(a) and 3(c). A Klocke Nanorobotics manipulator inside FEI Nova 200 dual beam FIB/SEM (Focused Ion Beam) setup was used for this purpose. While a bending radius of $560\ \mu m$ was achieved, the experiment was limited by concerns about damage to the tip of the manipulator.

Polydimethylsiloxane (PDMS) was used as a soft stamp to pick up the microprobe array and transfer-print it onto a planar or concave host substrate. An in-house micromanipulator setup was used to bring the microprobe array close to the host concave substrate. As interconnections and active Si islands are monolithically integrated, they all transferred in one step. Consequently, no alignment is necessary during the transfer-printing process, which facilitates much higher yield of complex circuits in comparison to competing technologies.[17] Figs. 3(b) and 3(d) show a $220\ \mu m$ diameter florescent microsphere coated with a thin PDMS layer ($50\ \mu m$) used as a host substrate for the transfer printing procedure. Conformal wrapping of the microelectrode onto a concave hemispherical florescent surface demonstrates the flexibility of the array with extremely small bending radius. CMOS sensors exhibited no change in their DC electrical performance after transferring.

A similar experimental method was also developed to transfer cells onto the surface of a microelectrode array. Figs. 4(a) and 4(b) illustrate optical and SEM images of a fixed mouse female germline stem cell transferred onto the microarray using a micro-tweezer. The operation mechanism of the micro-tweezer is reported elsewhere.[24,25] The stem

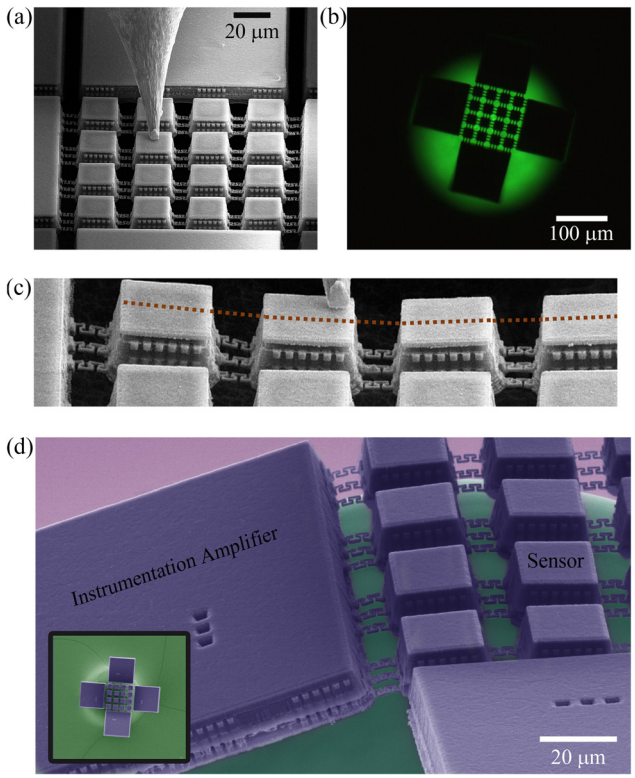

FIG. 3. (a) SEM micrograph illustrates the microelectrode array inside the FIB vacuum chamber. The tip is located on the surface of a micro island. (b) Fluorescent microscope image of the array laminating on a 220 μm fluorescent micro-bead. (c) SEM image illustrates the bent array under the Nanorobotic tip force. (d) False color SEM image of the microelectrode array transfer-printed on a florescent microsphere. Inset illustrates false color SEM image of the microelectrode array transfer-printed on a florescent microsphere.

cell is fixed in a 2.0% Gultaraldehyde in 0.1 M Cacodylate buffer pH 7.4 solution prior to transferring. Fig. 4(b) illustrates the false color SEM picture of the microelectrode array over a mouse ova. The extreme flexibility of the microelectrode array combined with the ability to transfer-print it on a curved surface facilitates extracellular recording of cell temperature and other vital signs.

In order to confirm the adaptability of the microelectrode array to the real cell environment, suspended microelectrode array was characterized under mechanical strain in a wet environment. Fig. 4(c) illustrates the schematic of the setup used for this experiment. In this experiment, a custom made micromanipulator setup was used to move a small pin in the Z direction, in order to gently deflect the suspended microelectrode array. The entire setup was placed under an optical microscope in order to facilitated pin alignment and imaging of the experiment. Figs. 4(d) and 4(e) illustrate the optical microscope image of the array before and after the array was deflected. Fig. 4(f) illustrates electrical measurement of the CMOS sensor in dry/wet and also in relaxed/strained conditions. Operation of the transistor is not affected by the strain of its environment.

A promising application of the microelectrode array is in single cell thermometry. CMOS temperature sensors can have high temporal resolution (fast response). In our experiment, the thermometer is based on buried CMOS transistors inside the islands. Note that in this experiment no live cell

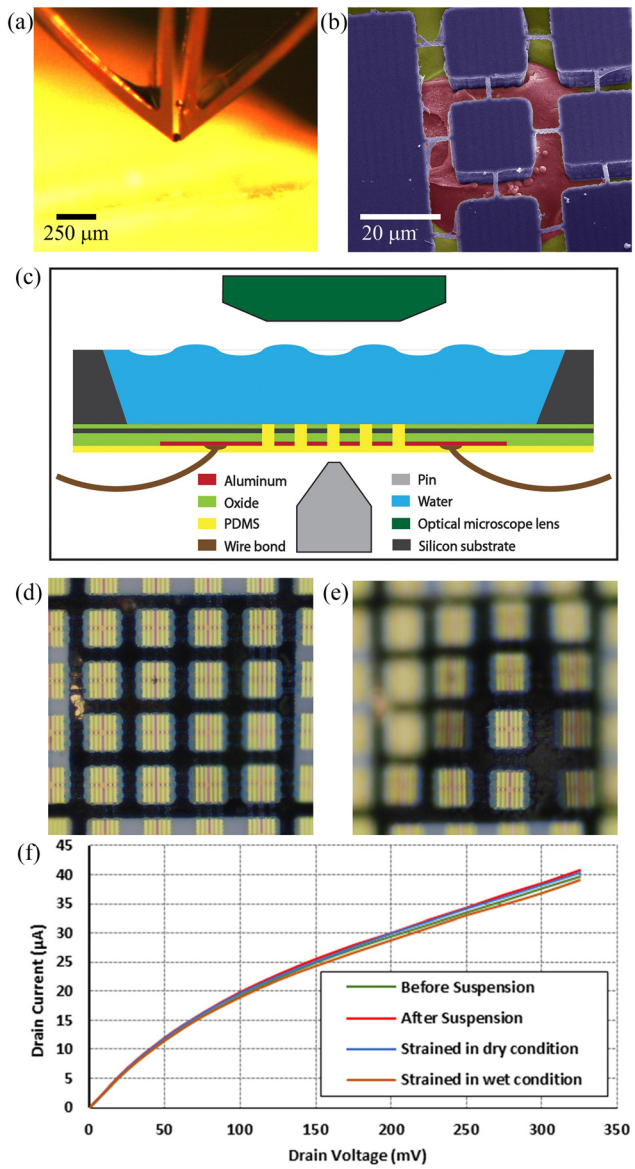

FIG. 4. (a) Optical image illustrating the cell manipulation onto the microelectrode array using a micro-tweezer. (b) SEM image of the microelectrode array covering a mouse female germline stem cell. (c) Schematic of the microelectrode array under strain and in wet condition. ((d) and (e)) Optical microscope image of the microelectrode array before applying the strain and under strain. (f) Experimental measurement of the FET's Drain current vs Drain voltage under different conditions.

was used and only the thermometer was calibrated. The DC electrical characteristics of CMOS transistors change by temperature variation. The CMOS sensor was calibrated using a hotplate by monitoring the CMOS transistor drain current as the temperature of the hotplate changes in the range of 35 °C–40 °C. First, the thermo-reflectance imaging microscopy[26] was used to confirm that the array elements are thermally isolated (Fig. 5(a)). The thermal isolation facilitates reading the temperature variation across a cell (or cells) without any influence from the environment (microelectrode array thermal path). To achieve maximum temperature sensitivity, the operation of the transistor was simulated under different biasing conditions to identify the most sensitive biasing region to temperature changes as illustrated in Fig. 5(b). This enabled us to exploit the linear dependence of drain current to temperature changes. Consequently, Gate-to-Source (Vgs) and

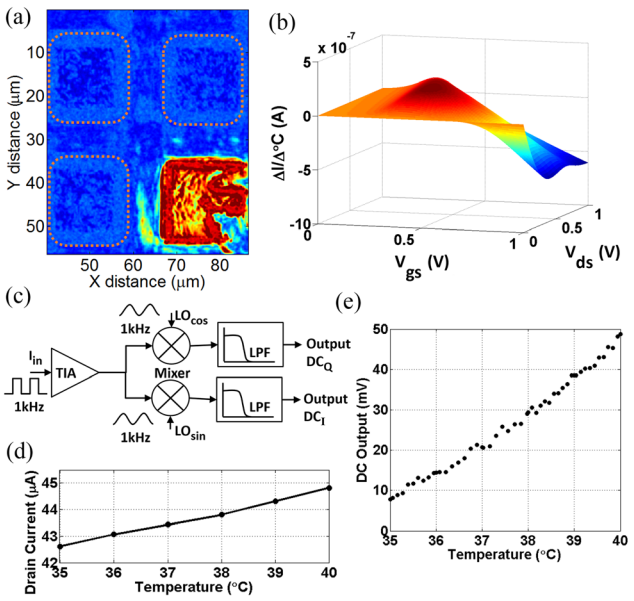

FIG. 5. (a) Thermal micrograph of four different islands captured using non-contact thermos-reflectance technique. In this image, the bottom right island is selectively heated up to evaluate thermal leakage among islands. (b) Computer modeling (Cadence virtuoso simulation) of the transistor indicating the most sensitive bias operation mode with respect to temperature. (c) Simplified schematic of the on-chip instrumentation amplifier design with an input transimpedance amplifier (TIA) and in-phase and quadrature mixers. ((d) and (e)) Measured temperature of the sensor in one of the islands (d) without lock-in amplifier in 1 °C steps and (e) with the integrated CMOS lock-in amplifier in 0.1 °C steps.

Drain-to-Source (Vds) voltages of the transistor were set to 400 mV and 300 mV, respectively, to achieve maximum temperature sensitivity at relatively small currents to avoid self-heating. Fig. 5(d) illustrates an average increase in the drain current of 370 nA/°C.

Fig. 5(c) shows a simplified schematic of the on-chip instrumentation amplifier, namely, a lock-in amplifier implemented in the 45 nm CMOS SOI process. The circuit is designed based on a Trans-impedance Amplifier (TIA) and two quadrature differential phase mixers. Transistor sizes are chosen to achieve small flicker noise. Fig. 5(e) shows the output voltage of the lock-in amplifier vs temperature. With an output voltage reading standard deviation of 425 μV, a temperature sensitivity of 0.15 °C is measured in this proof of concept design.

In summary, an ultra-flexible thermometer array based on ultrathin CMOS islands interconnected and hold together with meandered Cu metals is demonstrated. Unlike current extracellular recording techniques that are performed by electrodes from a distance of about 100 μm from the cell,[1] the developed microelectrode array conforms to the cell, facilitating an unprecedented access to "cellular information". Monolithic nature of silicon membranes and their meandered interconnections bypass the yield and signal integrity limitations of existing transfer-printed circuits.[17] The flexible microelectrode array enables simultaneous measurements at several sites, with direct contact to the cell surface. The use of a standard CMOS process and a simple post-processing technology that does not use any lithography combined with a one-step transfer-printing method has facilitated an important milestone for future flexible and stretchable electronics. The proposed technology can be used for flexible multi-functional sensing systems and may find a variety of applications including precision single-cell characterization, sensory skins, and smart wound therapy. These applications are emerged from conformal coverage of micro-curvatures combined with highly reliable and flexible complex integrated circuits achieved by the developed microelectrode array.

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